IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 – 30 (Cancelled)

31. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and ~~them~~then patterning by a lithography method.

32. (Previously Presented) The method of manufacturing a semiconductor device according to claim 31,

wherein said step (a) includes the step of forming second electrode pads having a side length of 20 μm or longer and comprised of said uppermost layer

wiring in said scribe region, and said step (c) includes the step of partially exposing a surface of said second electrode pad.

33. – 35. (Cancelled)

36. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 0.5 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

wherein a plurality of TEGs provided with said first electrode pads are formed in said scribe region, and

wherein, after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

37. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 1 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(b) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

wherein a plurality of TEGs provided with said first electrode pads are formed in said scribe region, and

wherein, after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

38. (Previously Presented) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said fist electrode pad, and then said TEG is measured.

39. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and rectangular second electrode pads having a side length of 20 μm or shorter each comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on aid first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to aid first electrode pad, and then said TEG is measured.

40. (Previously Presented) The method of manufacturing a semiconductor device according to claim 38,

wherein a plurality of TEGs provided with rectangular second electrode pads having a side length of 20 μm or longer and comprised of said uppermost layer wiring are also formed in the scribe region.

41. (Previously Presented) The method of manufacturing a semiconductor device according to claim 38,

wherein said first electrode pad is set formed so that the length of one side thereof is not longer than the dimension obtained by adding the diameter of a connection hole between said first electrode pad and the underlying wiring and the length of an alignment margin between said first electrode pad and said connection hole.

42. (Previously Presented) The method of manufacturing a semiconductor device according to claim 38,

wherein said first electrode pad is formed so that the length of one side thereof is about four-thirds of the diameter of a connection hole between said first electrode pad and the underlying wiring.

43. (Previously Presented) The method of manufacturing a semiconductor device according to claim 38,

wherein the surface of said first electrode pad is exposed in an island shape.

44. (Previously Presented) The method of manufacturing a semiconductor device according to claim 38,

wherein said protection film on said first electrode pad is removed by a focused ion beam method or a selective etching method.

45. (Previously Presented) The method of manufacturing a semiconductor device according to claim 39,

wherein said second electrode pad is connected commonly to the plurality of TEGs.

46. (Previously Presented) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming rectangular first electrode pads having a side length of 10 μm or shorter and rectangular second electrode pads having a side length of 20 μm or

shorter each comprised of an uppermost layer wiring in a scribe region and forming a bonding pad comprised of said uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad and a surface of said second electrode pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said first electrode pads and a plurality of TEGs provided with said second electrode pads are formed in said scribe region, and

after partially exposing the surface of said first electrode pad by removing said protection film on said first electrode pad, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said first electrode pad, and then said TEG is measured.

47. (Previously Presented) The method of manufacturing a semiconductor device according to claim 46,

wherein said second electrode pad is connected commonly to the plurality of TEGs.

48. (Previously Presented) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a bonding pad and an extraction electrode each comprised of an uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of TEGs provided with said extraction electrode are formed in said product circuit region, and

after partially exposing the surface of said extraction electrode by removing said protection film on said extraction electrode, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to said extraction electrode, and then said TEG is measured.

49. (Previously Presented) The method of manufacturing a semiconductor device according to claim 48,

wherein said protection film on said extraction electrode is removed by a focused ion beam method or a selective etching method.

50. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:

(a) forming a bonding pad and an extraction electrode each comprised of an uppermost layer wiring in a product circuit region;

(b) forming a protection film on an upper layer of said uppermost layer wiring; and

(c) partially exposing a surface of said bonding pad by removing a predetermined part of said protection film,

wherein said uppermost layer wiring is formed by depositing a conductive body and then patterning by a lithography method,

a plurality of logic circuits provided with said extraction electrode are formed in said product circuit region, and

after partially exposing the surface of said extraction electrode by removing said protection film on said extraction electrode, a probe having a tip radius of curvature of about 0.05 μm to 0.8 μm is contacted to ~~aid~~said extraction electrode, and then ~~said TEG is measured~~logic values of said logic circuits are evaluated.

51. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50;

wherein said protection film on said extraction electrode is removed by a focused ion beam method or a selective etching method.

52. (Previously Presented) The method of manufacturing a semiconductor device according to claim 50;

wherein said logic circuit comprises n input terminals and m output terminals, and n + m + 3 probes are contacted to said extraction electrodes to evaluate a logic value of said logic circuit.

53. (Previously Presented) The method of manufacturing a semiconductor device according to claim 52,

wherein one of said probes is a probe for contact confirmation.

54. (New) The method of manufacturing a semiconductor device according to claim 50,

wherein said probe contains tungsten as a main component.

55. (New) The method of manufacturing a semiconductor device according to claim 50,

wherein said logic circuits are TEG elements.

56. (New) The method of manufacturing a semiconductor device according to claim 36,

wherein said probe contains tungsten as a main component.

57. (New) The method of manufacturing a semiconductor device according to claim 38,

wherein said probe contains tungsten as a main component.

58. (New) The method of manufacturing a semiconductor device according to claim 39,

wherein said probe contains tungsten as a main component.

59. (New) The method of manufacturing a semiconductor device according to claim 46,

wherein the probe contains tungsten as a main component.

60. (New) The method of manufacturing a semiconductor device according to claim 48,

wherein the probe contains tungsten as a main component.